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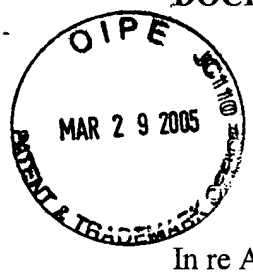

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Sailesh Merchant, *et al.*

Serial No.: 09/092,158

Filed: June 5, 1998

For: METHOD FOR THE FABRICATION OF CONTACTS IN AN INTEGRATED CIRCUIT DEVICE

Grp./A.U.: 2823

Examiner: Julio J. Maldonado

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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3-24-05 Marty Balko
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ATTENTION: Board of Patent Appeals and Interferences

Sirs:

APPEAL BRIEF UNDER 37 C.F.R. §41.37

This is an appeal from a Final Rejection dated February 17, 2005, of Claims 1, 4-12, and 15-24. The Appellants submit this Brief with the statutory fee of $500.00 for a large entity as set forth in 37 C.F.R.§41.20(b)(2), and hereby authorize the Commissioner to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §41.37(c)(1):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

IV. STATUS OF AMENDMENTS

V. SUMMARY OF CLAIMED SUBJECT MATTER

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

VII. APPELLANTS' ARGUMENTS

VIII. APPENDIX A - CLAIMS

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Agere Systems Inc.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1 and 4-11, Claims 12 and 15-23, and Claim 24 are pending in this application and have been rejected under 35 USC § 103. The rejection of each of the pending claims is being appealed.

IV. STATUS OF THE AMENDMENTS

The Appellants wish to note for the record that this is the third appeal brief that the Appellants have been compelled to file in this case. The present Application was filed on June 5, 1998. Since the first Appeal Brief filed in November 11, 2000, the Appellants have responded to eight Office Actions issued by the Examiner, including three Final Rejections that were subsequently withdrawn. In response to a fourth Final Rejection issued in an Office Action mailed February 12, 2004, the Appellants filed a Request for Reconsideration on March 15, 2004 with no amendments to the Claims. The Examiner issued an Advisory Action on April 2, 2004 indicating that the March 15, 2004 reply failed to put the application in condition for allowance. The Appellants filed a Notice of Appeal on April 26, 2004 and Appellants filed a second Appeal Brief on November 22, 2004. In an

Office Action mailed August 25, 2004 the Examiner once again withdrew the Final Rejection with respect to dependent claims 4 and 15, but the Examiner then rejected these claims again on the same basis as for the other claims as set forth previously in the fourth Final Rejection of February 12, 2004. On November 22, 2004 the Appellants responded to the Office Action of August 25, 2004 by filing a Request for Reconsideration with no amendments to the Claims. The Examiner issued a fifth Final Rejection on February 17, 2005, stating the same basis for rejecting the Claims as set forth in the fourth Final Rejection of February 12, 2004. The Appellants filed a Notice of Appeal on March 18, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed, in general, to a method of fabricating contact plugs, and more specifically, to a method of fabricating tungsten plugs in an integrated circuit device. The present invention provides a method of forming a tungsten plug that exhibits improved contact resistance characteristics in the window provided by a thermal anneal without inducing failure of the titanium nitride layer. In general, and as presently amended, the present invention is directed to a method for fabricating a contact in a semiconductor substrate. In a claimed embodiment, the method includes depositing, by physical vapor deposition, a barrier layer in a contact opening 410 and on at least a portion of the semiconductor substrate 400 (Page 14, Line 4 to Page 17 Line 16). Depositing the barrier layer includes depositing a titanium layer 414 and depositing a titanium nitride layer 415 on the titanium layer 414 such as shown in FIGURE 4 (illustration 1 presents FIGUREs 4 and 5).

FIG. 4

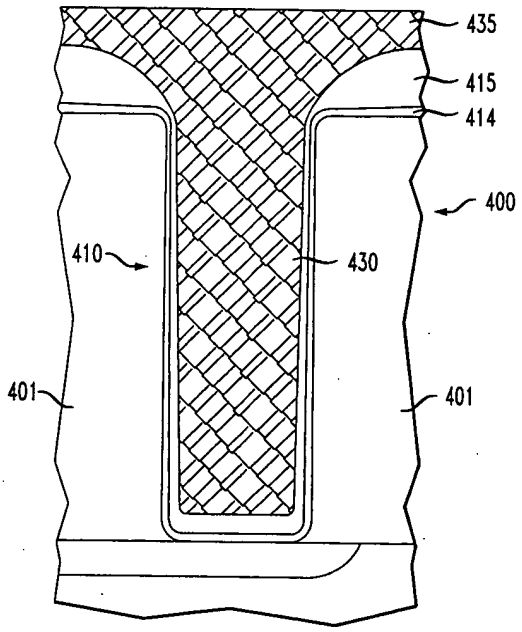

FIG. 5

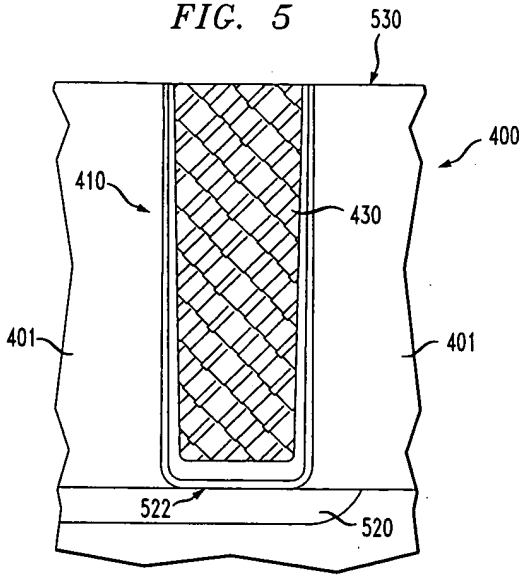

Illustration 1

The method also includes depositing a contact metal 435 on the barrier layer 414, 415 within the contact opening 410, also shown in FIGURE 4. A substantial portion of the contact metal 435 and the barrier layer 414, 145 is removed from the semiconductor substrate to form a contact plug 430 within the contact opening 410, with the plug 430 extending to an uppermost surface 530 of the substrate, such as shown in FIGURE 5. The contact plug 430 is then subject to a temperature from about 600°C to about 750°C to anneal the barrier layer. It is important to note that the contact plug 430 is subject to this temperature range after the removal process. Importantly, this process sequence avoids the damaging effects of thermal anneals done immediately after the deposition of the titanium layer 414 and titanium nitride layer 415 (Appellants' Specification, Page 10, Lines 11-15).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issue presented for consideration in this appeal is whether Claims1, 5-11, 12 and 16-23 and 24 as rejected by the Examiner are patentably nonobvious in accordance with 35 U.S.C. §103(a) over U.S. Patent No. 5,591,671 to Kim *et al.* (hereinafter "Kim") in view of U.S. Patent No. 5,714,418 to Bai *et al.* (hereinafter "Bai") and U.S. Patent No. 5,970,374 to Teo (hereinafter "Teo").

VII. APPELLANTS' ARGUMENT

For the reasons set forth below, the invention recited in Claims1, 5-11, 12 and 16-23 and 24 are not made obvious by the reference applied by the Examiner.

A. Kim.

Kim is directed to a method for interconnecting layers in a semiconductor device, which can form a low resistance contact (Kim, Abstract). A titanium ohmic contacting layer and a titanium nitride barrier layer are formed in the interior of an opening hole and on an insulating layer in sequence (Kim, Abstract). Thereafter, a refractory metal layer is formed which completely fills the remainder of the opening hole by depositing the refractory metal on the barrier layer (Kim, Abstract). To improve a contacting property, the resultant structure is heat-treated at a temperature above 450°C (Kim, Abstract). Kim states that it is desirable that the heat treatment be performed at a high temperature of about 500°C (Kim, Column 2, Line 9-11). Kim, however, is also concerned with preventing oxidation of his ohmic contact and barrier layers when heated at a temperature of about 500°C because this deteriorates their contact resistance due to oxide formation (Kim, Column 2, Lines 8-22). Kim states that this phenomenon is severe when the heat treatment temperature is

above 500°C (Kim, Column 2, Lines 18-19). To reduce oxidation, Kim deposits the refractory metal layer 28 on the whole surface of the structure shown in FIGURE 2D, and then heats the resultant structure shown in FIGURE 2E (both FIGUREs 2D and 2E of Kim are presented in illustration 2) at a temperature above 450°C, and more preferably at 500°-550°C (Kim, Column 4, Lines 62-64). Among the several examples given by Kim, heating beyond 550°C is never disclosed or suggested (*see, e.g.*, Kim, Column 6, Lines 18-24).

FIG. 2D

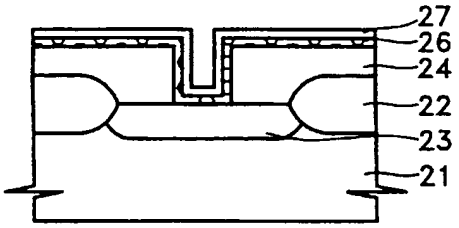

FIG. 2E

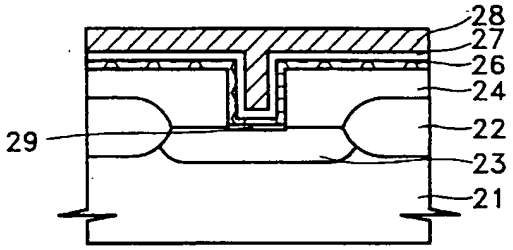

Illustration 2

In another embodiment, the refractory metal 28, ohmic contact layer 26 and barrier layer 27 on insulating layer 24 is etched-back, thereby leaving the metal only in the contact hole (Kim, Column 5, Lines 61-66), as shown in Kim's FIGURE 4B (illustration 3). The metal 28 is etched back *below* the level of the substrate to accommodate the deposit of an oxidation preventing cap layer 34 (Kim,

Column 5, Line 66-67), shown in Kim's FIGURE 4C (illustration 3). Thereafter, the resultant structure is heated (Kim, Column 6, Line 1-3).

FIG. 4B

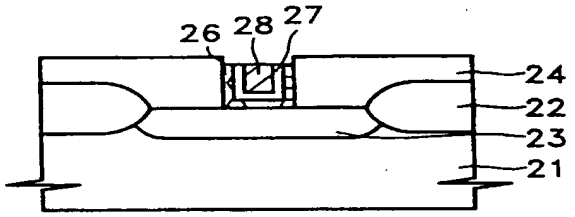

FIG. 4C

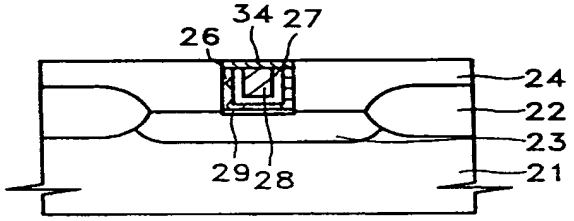

Illustration 3

B. Bai.

Bai is directed to an electrical interconnect structure with a bi-layer diffusion barrier, comprising a capturing layer beneath a blocking layer, and a method of forming the structure over a semiconductor substrate (Bai, Abstract). After forming capture layer 43 and blocking layer 42, as shown in Bai's FIGURE 4B (illustration 4 presents FIGUREs 4B-4D of Bai), but before depositing the conductive layer of copper, Bai subjects the bi-layer diffusion barrier to an optional high temperature process step to anneal the barrier at 500°C (Bai, Column 8, Lines 58-64).

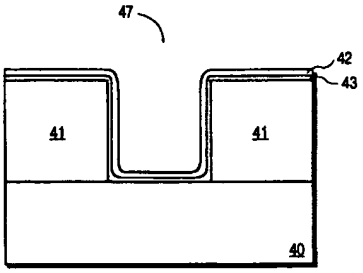

FIG. 4B

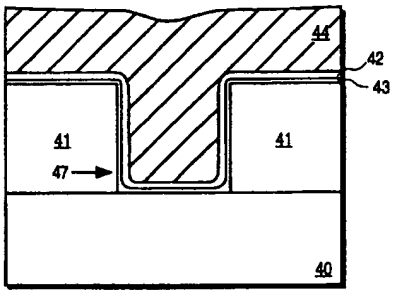

FIG. 4C

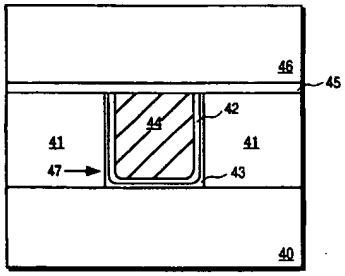

FIG. 4D

Illustration 4

Bai does this to anneal micro defects in the barrier layer so that the barrier layer can be more effective in preventing diffusion of Copper atoms into the device (Bai, Column 3, Lines 56-66, and Column 8, Lines 63-65). Subsequently, as shown in Bai's FIGURE 4C, Bai deposits a copper layer 44 (Bai, Column 9, Lines 4-11). Later, Bai performs a chemical mechanical polishing (CMP) process to remove the copper layer 44, blocking layer 42 and capturing layer 43 from the upper surface of the dielectric layer (41) (Bai, Column 9, Line 12-19, and FIGURE 4D). There is no teaching or suggestion of performing a thermal anneal after the CMP process.

C. **Teo.**

Teo is directed to a method for forming void-free, low resistance tungsten plug contacts and vias within openings having a Ti-TiN metallurgy deposited by PVD techniques, such as sputtering (Teo, Column 3, Lines 15-19). Teo deposits a Ti layer 16 and a TiW layer 18 (Column 4, Lines 17-22) into an opening as shown in FIGURE 3A (see illustration 5, presenting FIGUREs 3A-3F of Teo) and then subjects this structure to an optional rapid thermal anneal of 670°C for 30 seconds (Teo, Column 4, Lines 17-22). Teo then partially fills the contact opening with spin-on-glass, SOG 26 (Teo, Column 4, Lines 33-48; FIGURE 3B). Teo next performs CMP until the final design thickness 24 is reached (Teo, Column 4, Lines 49-58, and FIGURE 3C), and then removes the SOG 26 (Teo, Column 4, Lines 59-63, and FIGURE 3D). After depositing a barrier layer 30, tungsten 40 is deposited in the opening and then etched back to define the tungsten plug 42 (Teo, FIGUREs 3E-3F,and Column 4, Line 64 to Column 5, Line 15).

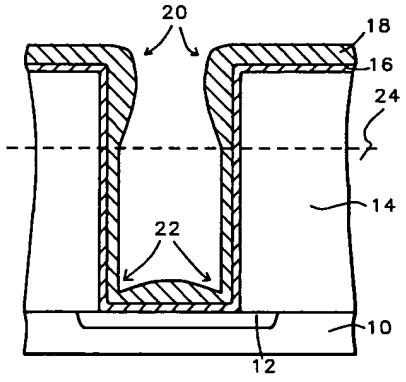

FIG. 3A

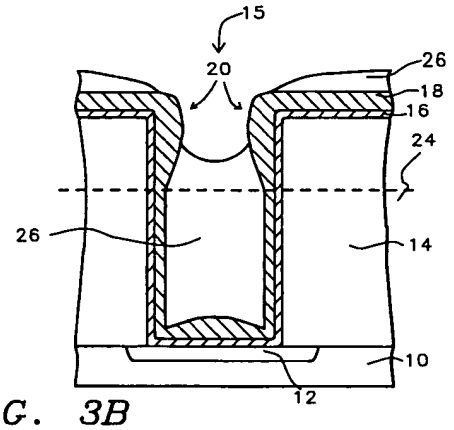

FIG. 3B

Illustration 5

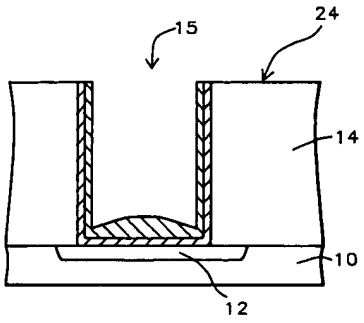

FIG. 3C

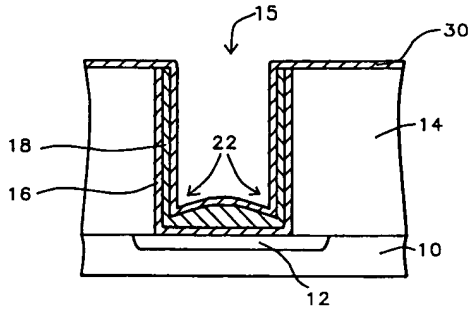

FIG. 3D

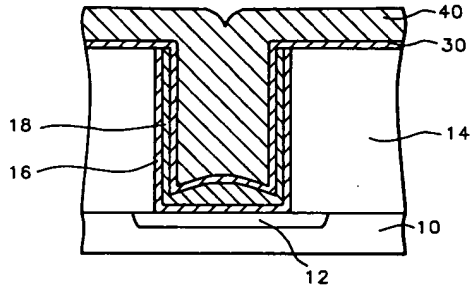

FIG. 3E

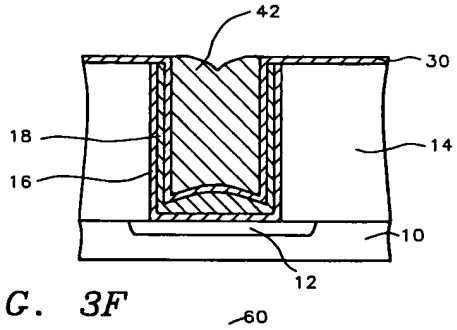

FIG. 3F

Illustration 5 (continued)

D. Kim and Bai are not properly combinable.

The Examiner acknowledges that Kim fails to show extending a plug to an uppermost surface of the substrate (Page 5 of Examiner's Office Action mailed February 12, 2004; Page 3 of Examiner's Office Action mailed February 17, 2005). The Examiner relies on Bai, referring to FIGUREs 4C-4D of Bai (illustration 4), for the proposition of teaching the steps of removing a substantial portion of a contact metal (44) and barrier layer (42,43) from a semiconductor substrate (40,41) to form a contact plug within a contact opening (47), the plug extending to an uppermost surface of the substrate (40,41). The Examiner believes one of ordinary skill in the art would be motivated to enable the removing step of Kim to be performed according to Bai because this would isolate the interconnect

layer within the trench. Citing MPEP 2144.07, the Examiner further states that one would look to alternative suitable methods of performing the removing step of Kim that are recognized as suitable for an intended purpose. The Appellants respectfully disagree that Bai's removing step is a suitable alternative method for Kim's process. Because of the disparate teachings of Kim and Bai, one skilled in the art would not be motivated to combine Bai's removing step in Kim's process.

It is well established that to establish a *prima facie* case of obviousness, three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. See MPEP §2143 - §2143.03 for decisions pertinent to each of these criteria.

As is well settled, "[o]bviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572,1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The case law also makes clear that one "cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *Ecolochem, Inc. v. So. California Edison*, 56 USPQ2d 1065, 1073 (Fed. Cir. 2000), *In re Fine*, 837 F.2d 1071,1075, 5 USPQ2d 1780, 1783 (Fed. Cir. 1988). Hindsight knowledge of the Applicants' disclosure when the prior art does not teach or suggest such knowledge, results in the use of the invention as a template for its own reconstruction. This is inappropriate in the determination of

patentability. *Sensonics Inc. v. Garlock, Inc.*, 220 USPQ 303, 312-313 (1983). Moreover, where the inventor has achieved the claimed invention by doing what those skilled in the art suggested should not be done is a fact strongly probative of nonobviousness. *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 19860, on rehearing, 231 USPQ 160 (Fed. Cir. 1986).

First, the Appellants wish to note that the section of the MPEP 2144.07 cited by the Examiner presents case law which discusses the *selection of known materials* based on their suitability to support a *prima facie* obviousness determination, and not the *selection of known methods*. The Appellants submit that extending MPEP 2144.07 to methods goes beyond the supporting case law.

Second, the Appellants submit that one skilled in the art would not be motivated to incorporate Bai's removing method into Kim's removing step in the manner suggested by the Examiner because i) there is no suggestion or motivation in the references themselves to support their combination and ii) there is not a reasonable expectation of success. Introducing new, or switching, steps in a process, such as a process flow for semiconductor fabrication, can have unpredictable consequences and therefore a change in a process flow is not done without a strong motive to do so.

As noted above, Kim performs a heat treatment after depositing the refractory metal layer 28 on the whole surface of the structure shown in Kim's FIGURE 2D, or after etching back the metal 28 to be only in the opening and then forming a protective oxidation cap 34 over the metal plug 28 in the opening, as shown in Kim's FIGURE 4C. Kim does this to avoid the deleterious effects of oxidation of the ohmic contact and barrier layers during the heat treatment. Clearly Kim does not wish to use a removing step that would result in either the ohmic contact or the barrier layers being oxidized during the heat treatment

However, this is what would occur if one were to use Bai's CMP method to remove a substantial portion of a contact metal and barrier layer from a semiconductor substrate, instead of Kim's method of etching back followed forming a protective oxidation cap 34. Therefore Bai's removing step is not suitable for use in Kim process flow, because it would expose portions of Kim's barrier layer to oxidation during thermal annealing, which Kim expressly wishes to avoid. Therefore, contrary to the Examiner's proposal, Bai's method is not a suitable alternative method for Kim's purpose.

In response to this argument, in an Office Action mailed Aug 25, 2005, the Examiner cited Column 5, Lines 24-42 of Kim. This section of Kim indicates that after forming the refractory metal layer as described with respect to FIG. 2E, the refractory metal layer is patterned together with a barrier layer and an ohmic contacting layer 26, which are laminated on an insulating layer, thereby forming a metal pattern. The Examiner further states that Kim "is silent as to the form of this pattern." But from this, the Examiner concludes that Kim and Bai "demonstrate a plug with an uppermost portion extending to the surface of the substrate as recited in Claim 1 can be obtained."

In response, the Appellants maintain that the issue is not what "can be obtained," but whether there is a suggestion or motivation to modify Kim according to Bai and that there is a reasonable expectation of success. The Appellants submit that the above-cited section of Kim does not provide one of ordinary skill in the art with motive to enable the removing step of Kim to be performed according to Bai. As pointed out above, Kim wants to avoid the deleterious effects of oxidation of the ohmic contact and barrier layers during thermal annealing, but Bai's CMP method would expose portions of Kim's barrier layer to oxidation during thermal annealing. Nor is there a reasonable

expectation of success, given Kim's disclosure concerning the occurrence of oxidation induced severe deterioration of contact resistance at temperatures above 500°C.

E. Kim in view of Bai and Teo fail to teach or suggest all elements of the claimed invention.

The Examiner also acknowledges that the combined teachings of Kim and Bai do not teach performing heating in the temperature range from about 600°C to about 750°C to anneal the barrier layer (Page 3 of Examiner's Office Action mailed February 12, 2004; and Page 3 of Examiner's Office Action mailed February 17, 2005). To remedy the deficient teachings of Kim and Bai, the Examiner relies on Teo. The Examiner states that it would be obvious to one of ordinary skill in the art to use the rapid thermal anneal process taught by Teo in the combination of Kim in view of Bai because this improves the adhesion of the barrier layer in the contact layer.

The Appellants respectfully submit that even with the addition of Teo, this combination of references still does not teach or suggest the element of subjecting a contact plug, as defined in Appellants' Claim 1, to the above temperature range to anneal the barrier layer.

Claim 1 recites that the contact plug is within the contact opening, the plug extending to an uppermost surface of the substrate. Therefore, the contact plug that is subjected to a temperature from about 600°C to about 750°C is a plug that extends to the uppermost surface of the substrate. Neither Kim, Bai, nor Teo, whether taken alone or in combination, disclose subjecting such a contact plug to this temperature range.

As noted above, Kim performs a thermal anneal on the structure shown in Kim's FIGURE 2E, after depositing the refractory metal layer 28 on the whole surface of the structure shown in Kim's FIGURE 2D. Alternatively, Kim performs a heat treatment only after both i) etching back the metal 28 to be only in the opening and ii) forming a protective oxidation cap 34 over the metal plug

28 in the opening, as shown in Kim's FIGURE 4C. Therefore, neither of the structures shown in FIGURE 2E or FIGURE 4C that are heated by Kim have a contact plug as defined in Claim1. This follows because neither of Kim's structures have plugs that extend to an uppermost surface of the substrate. In the structure shown in FIGURE 2E, the refractory metal layer 28 extends beyond the uppermost surface of the substrate, while in the structure shown in FIGURE 4C, the metal 28 is below the uppermost surface of the substrate. Therefore, Kim does not teach heating a contact plug that extends to an uppermost surface of the substrate, as recited in Appellants' Claim 1.

Bai performs a high temperature process step after forming the bi-layer diffusion barrier of the capture layer 43 and blocking layer 42, shown in Bai's FIGURE 4B, but before depositing the conductive layer of copper. As noted above, Bai does this to cure micro defects so that the barrier layer can be more effective at preventing diffusion of copper atoms into the device. Therefore, Bai also does not teach subjecting a contact plug as defined in Claim 1 to an elevated temperature.

It follows, therefore, that the Examiner must rely on Teo, not only for teaching heating to a specific temperature range, but also for teaching the subjecting a contact plug as defined in Claim 1 to this temperature range.

Teo, however, does not disclose subjecting such a contact plug to an elevated temperature. Rather, Teo indicates that it is the structure shown in Teo's FIGURE 3A that can be subjected to the optional rapid thermal anneal of 670°C for 30 seconds (Teo, Column 4, Lines 17-22). The structure shown in FIGURE 3A, however, does not have a contact plug. Rather, the opening shown in FIGURE 3A is not filled with tungsten until Teo's process flow has progressed to the stage shown in Teo's FIGURE 3D. Thus, Teo, as with Kim and Bai, does not teach or suggest subjecting a contact

plug extending to the uppermost surface of the substrate to the specified temperature range recited in Appellants' Claim 1.

In response to this argument, the Examiner has stated that Teo was relied on for disclosing a specific annealing process not the actual annealing process at some point in the process (Page 7 of Examiner's Office Action mailed February 12, 2004; Page 6 of Examiner's Office Action mailed February 17, 2005).

Even if this is the case, the combination of Kim in view of Bai and Teo still fails to teach or suggest all elements of the process recited in Claim 1 because these references fail to teach or suggest subjecting the contact plug as defined in Claim 1 to the recited temperature range.

F. Teo is not properly combinable with Kim.

Teo is not properly combinable with Kim because one of ordinary skill in the art would not be motivated to use Teo's annealing temperature in Kim's heat treatment. Kim is concerned with preventing oxidation of his ohmic contact (*e.g.* Ti) and barrier (*e.g.*, TiN) layers when heated at a temperature of above 500°C, because this severely deteriorates their contact resistance (Kim, Column 2, Lines 8-22). To reduce oxidation, Kim deposits the refractory metal layer 28 on the whole surface of the structure shown in FIGURE 2D and then heats the resultant structure shown in FIGURE 2E at a temperature above 450°C, and more preferably, at 500°-550°C. As noted above, Kim does not disclose or suggest heating beyond 550°C.

In contrast, Teo's optional rapid thermal anneal (RTA) at 670°C is done *after* the deposition of a Ti layer 16 and a TiW layer 18 (Teo, Column 4, Lines 17-25; FIG. 3A), but *before* the deposition of tungsten 40 (Teo, Column 5, Lines 3-8; FIGURE 3E). Thus Teo's RTA is conducted at a much earlier point in the fabrication process than the heating step used in Kim's process.

The Appellants maintain that there is insufficient motive for one skilled in the art to apply Teo's RTA of 670°C to the heat treatment in Kim's process. The Examiner seeks to use Teo's statement that RTA activates the carriers in the silicon and forms strong chemical bonds to the Ti as the motive for inserting Teo's RTA into Kim's process. Kim, however, is trying to balance the benefits of heating above 450°C to improve the interconnection properties of the ohmic contact and barrier layers (Kim, Column 1, Lines 60-62), against severe oxidation of these layers at temperatures above 500°C (Kim, Column 2, Lines 13-22). Even with his refractory metal layer 28 in place, however, Kim is careful not to heat beyond 550°C. Based on these considerations there is no reason why one skilled in the art would be motivated to heat Kim's ohmic contact and barrier layers beyond Kim's limit of 550°C, using Teo's teaching of performing a RTA on Ti and TiW layers in an *unfilled* contact opening 15 shown in Teo's FIGURE 3A. Moreover, because Teo's RTA is conducted at a different point in the fabrication process than Kim's heating step, one skilled in the art would be extremely reluctant to change Kim's heating step to Teo's RTA. Given that Kim uses temperatures up to 550°C, one skilled in the art would not have motive to change the heating step to 600°C and beyond as done by Teo.

In response to this argument the Examiner has reiterated that Teo's teaching that an RTA improves adhesion of the barrier layer in the contact opening provides motive for this combination of references (Page 7 of Examiner's Office Action mailed February 12, 2004; Page 7of Examiner's Office Action mailed February 17, 2005). The Examiner has also argued that Kim is open to performing Teo's heating process because Kim is silent as to the type, duration and temperature and is open to heating at temperatures above 450°C (Page 7 of Examiner's Office Action mailed August 25, 2004).

As the Appellants have pointed out to the Examiner (Response filed November 22, 2004), Kim is not silent about his heating process. Rather, Kim presents experimental data in Fig. 5, Table 1, and at Column 6, Lines 18-45, that describes the durations of heating, the temperatures used, and when the heat treatment is performed. Among the several examples given by Kim, heating beyond 550°C and for shorter than 10 minutes is never disclosed or suggested. Furthermore, as indicated in Table 1 of Kim, heating is done *after* metal layer formation, not *before*, as done by Teo.

The Appellants submit that one of ordinary skill in the art would not be motivated to use Teo's teaching of doing an RTA on Ti and TiW layers in an unfilled contact opening 15 in Kim's process, given Kim's teaching of avoiding severe oxidation of the ohmic contact and barrier layers at high temperatures (Kim, Column 2, Lines 13-22). As noted above, Kim expressly discloses the importance of balancing the benefits of heating above 450°C to improve the interconnection properties of the ohmic contact and barrier layers (Kim, Column 1, Lines 60-62), against the oxidation of these layers and the severe deterioration of their contact resistance at temperatures above 500°C (Kim, Column 2, Lines 13-22). Moreover the fact that Teo's RTA step is conducted at a different point in the fabrication process than Kim's heating step, provides one of ordinary skilled in the art with even less motivation to change Kim's heating step to Teo's RTA step.

G. Conclusion.

In conclusion, because the references of Kim in view of Bai and Teo do not teach or suggest all elements of the present invention and are not properly combinable, the Examiner has failed to establish a *prima facie* case of obviousness with respect to Appellants' independent Claim 1. A similar conclusion applies to independent Claim 12 and 24, which contains elements analogous to that discussed for Claim 1 above. Accordingly, the Appellants respectfully request that the Board of

Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claims 1, 12 and 24 and their respective dependent claims.

For the reasons set forth above, the Claims on appeal are patentably nonobvious over Kim in view of Bai and Teo. Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of all of the Appellant's pending claims.

Respectfully submitted,

Hitt Gaines, P.C.

Ronald J. Corbett
Registration No. 47,500

Dated: 3-24-05

Hitt Gaines, P.C.
P.O. Box 832570
Richardson, Texas 75083-2570
(972) 480-8800
(972) 480-8865 (Fax)
ron.corbett@hittgaines.com

VIII APPENDIX A - CLAIMS

1. A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing by physical vapor deposition a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate; and

subjecting said contact plug to a temperature from about 600°C to about 750°C to anneal said barrier layer.

4. The process of Claim 1 wherein said depositing said barrier layer includes depositing said barrier layer in said contact opening formed in a dielectric and having an aspect ratio ranging from about 3:1 to about 5:1.

5. The process of Claim 1 wherein said depositing a contact metal includes depositing tungsten.

6. The process of Claim 5 wherein said depositing includes depositing said tungsten by chemical vapor deposition.

7. The process of Claim 1 wherein said subjecting includes subjecting said contact plug to a rapid thermal anneal process.

8. The process of Claim 1 wherein said depositing a barrier layer includes forming a thickness of said barrier layer ranging from about 5 nm to about 20 nm within said contact opening and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater.

9. The process of Claim 8 wherein said thickness of said barrier layer within said contact opening is about 5% to about 20% of said field area thickness.

10. The process of Claim 8 wherein removing a substantial portion includes removing said contact metal and said barrier layer from said field area thickness.

11. The process of Claim 10 wherein said removing said contact metal and said barrier layer includes removing said contact metal and said barrier layer by chemical/mechanical polishing processes.

12. A process for fabricating an integrated circuit, comprising:

forming an active device on a semiconductor substrate;

forming a contact opening in a dielectric deposited on said active device, said contact opening in electrical contact with said active device;

depositing by physical vapor deposition a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate; and

subjecting said contact plug to a temperature from about 600°C to about 750°C to anneal said barrier layer.

15. The process of Claim 12 wherein said forming said contact opening includes forming said contact opening having an aspect ratio ranging from about 3:1 to about 5:1.

16. The process of Claim 12 wherein said depositing a contact metal includes depositing tungsten.

17. The process of Claim 16 wherein said depositing includes depositing said tungsten by chemical vapor deposition.

18. The process of Claim 12 wherein said subjecting includes subjecting said contact plug to a rapid thermal anneal process for a period ranging from about 5 seconds to about 60 seconds.

19. The process of Claim 12 wherein said depositing a barrier layer includes forming a thickness of said barrier layer ranging from about 5 nm to about 20 nm within said contact opening and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater.

20. The process of Claim 19 wherein said thickness of said barrier layer within said contact opening is about 5% to about 20% of said field area thickness.

21. The process of Claim 19 wherein removing a substantial portion includes removing said contact metal and said barrier layer from said field area thickness.

22. The process of Claim 21 wherein said removing said contact metal and said barrier layer includes removing said contact metal and said barrier layer by chemical/mechanical polishing processes.

23. The process of Claim 12 wherein forming said active device includes forming an active device having a design width of about 0.25 microns or less.

24. A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate; and

subjecting said contact plug to a temperature from about 600°C to about 750°C to anneal said barrier layer.

PTO/SB/92 (09-04)
Approved for use through 07/31/2006. OMB 0561-0031
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